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Claims

1. A method of converting analog electric signals into a stream of binary data, comprising the steps of:

    (a) Comparing the input analog signal with a predefined threshold value,

    (b) Triggering a transition pulse when the input signal reaches said predefined threshold value,

    (c) Digitally monitoring the occurrence of a transition pulse to command starting of a new comparison step.

2. The method of claim 1, wherein the input signals consist of a finite amount of charge stored in a charge reservoir.

3. The method of claim 1, wherein the input signals consist of voltage signals.

4. The method of claim 1, implemented in one circuitry arranged to receive input signals consisting of finite amounts of charge and voltage signals.

5. The method of claim 1, implemented in a circuitry including devices fabricated using purely digital CMOS process technology.

6. The method of Claim 1, implemented in a circuitry including digital CMOS devices and wherein the total bandwidth of the ADC is tightly coupled to the intrinsic performance of the digital CMOS devices.

7. The method of claim 2, implemented in a circuitry including devices fabricated using purely digital CMOS process technology.

8. The method of Claim 2, implemented in a circuitry including digital CMOS devices and wherein the total bandwidth of the ADC is tightly coupled to the intrinsic performance of the digital CMOS devices.

9. The method of claim 3, implemented in a circuitry including devices fabricated using purely digital CMOS process technology.

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10. The method of Claim 3, implemented in a circuitry including digital CMOS devices and wherein the total bandwidth of the ADC is tightly coupled to the intrinsic performance of the digital CMOS devices.

5   11. The method of claim 4, implemented in a circuitry including devices fabricated using purely digital CMOS process technology.

12. The method of Claim 4, implemented in a circuitry including digital CMOS devices and wherein the total bandwidth of the ADC is tightly coupled to the intrinsic performance of the digital
10   CMOS devices.

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